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MICROMINIATURE LAYERED PRINTED WIRING

Signal Corps Contract Number DA-36-039-SC-90763

2nd QUARTERLY REPORT

15 September 1962

to

15 December 1962

REPORT No. 2

DEPARTMENT OF THE ARMY PROJECT NO. 3A99-15-002
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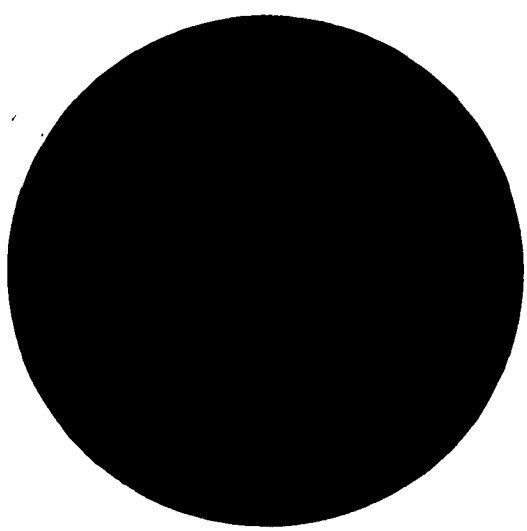

Photocircuits
CORPORATION
GLEN COVE, NEW YORK

U.S. Army Electronics Research and Development Laboratory

Fort Monmouth, New Jersey

MICROMINIATURE LAYERED PRINTED WIRING

2nd Quarterly Report
Report #2

15 September 1962 to 15 December 1962

The object of this contract is research work directed toward the development of Microminiature Layered Printed Wiring to interconnect Microassemblies.

Signal Corps Contract No.	DA-36-039-sc-90763
Signal Corps Specification	SCL 7653 27 November 1961
Department of the Army Project No.	3A99-15-002
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SECTION 1

PURPOSE

1.0 OBJECTIVES

The objective of this contract is to develop Flush Terminated Microminiature Layered Printed Wiring suitable for assembling and electrically interconnecting electronic module leads located on 0.050" centers by a single soldering operation. This Layered Printed Wiring must provide reliable interlayer connection between conductors of any layers and should withstand the military environment defined in SCL-7653 specification.

2.0 PHASES OF WORK

Chronologically, the work on this contract is divided into three phases:

Phase 1 - Preliminary Research & Development work

This phase will cover the preliminary research and development work required to establish certain process parameters for the manufacture of Microminiature Layered Printed Wiring, with plated-through holes as the interconnecting link between layers. During this phase the following tasks are to be accomplished:

a) Investigation of thin conductor etching.

b) Investigation of laminating cycles and of the tooling needed to minimize misregistration between layers during lamination.

c) Investigation of procedures for accurate drilling of small diameter holes.

d) Investigation of a satisfactory hole metallizing system.

e) Establish parameters for reliable miniature plated through holes.

f) Establishment of Quality Assurance procedures for the entire process with special emphasis on plated-through holes.

g) Preparation of artwork for the production of samples to meet the requirements of SCL 7653 specification.

Phase II - Process & Design Parameters

In this phase the results of first phase will be evaluated. Based on this evaluation, the processes will be standardized and production specifications, design parameters and tooling design for the production of the final samples will be prepared and the samples manufactured. The Quality Control standards and detailed testing schedules for sample testing will be prepared in this phase. The completion of these tasks is expected by the end of February 1963.

Phase III - Testing of Samples

This phase will be devoted completely to the testing of the samples under environmental conditions specified in SCL 7653. At the latter part of this phase, the procurement specifications will be prepared for inclusion in the final report. The completion of this phase will coincide with the end of the subject contract.

3.0 RELATED PROJECTS

Photocircuits Corporation has a U.S. Army Signal Corps contract for Production Engineering Measure for Subminiature and Ultra-miniature Multilayer Printed Wiring.

Information or data obtained during the work on this contract which is pertinent to the outlined tasks of the subject contract will be included in the interest of completeness.

SECTION 2

ABSTRACT

In the period covered by this report further investigations were carried out in the preliminary research and development phase of the contract.

Additional data on the etching of thin conductors has been collected, the tolerance limitations and the shapes of the crossections of the thin etched conductors have been established. The parameters of the variables of the lamination cycle have been determined. The placing of resilient layers between the circuit stack and the jig plates for even pressure distribution during lamination, has been found desirable. The laminating plates must be manufactured of materials which are stable under repetitive temperature and pressure cycling. A technique for registration of all layers within ± .003" from true position has been developed.

The drilling of small holes in ultraminiature layered printed wiring must be a tightly controlled process in order to obtain uniform clean holes. The use of upside down drilling machines has made it possible to keep the required tolerances on hole locations.

Uniform copper deposition can be achieved in holes with diameters less than .025" and more than two diameters deep when panel plating technique is used. For plating of such holes in circuit boards without any circuit patterns or bands on either surface, special techniques must be developed.

SECTION 3

PUBLICATIONS, LECTURES, REPORTS AND CONFERENCES

During the period covered by this report, no lectures have been given, or reports published which include any material or data from the work performed under this contract.

The following conferences were held between representatives of the U. S. Army Electronics Research and Development Laboratory and Photocircuits Corporation to discuss technical progress of work done under this contract:

1. September 27, 1962 at Fort Monmouth, N. J.
2. November 19, 1962 at Fort Monmouth, N. J.

SECTION 4

FACTUAL DATA

4.1 THIN CONDUCTOR ETCHING

4.1.1 Objectives of this Task

The objectives of this task are to determine:

a. The minimum conductor width which can be manufactured using standard production equipment.

b. The relationship of conductor widths on photoprint glass negatives to the width of conductors on etched parts.

4.1.2 Background

In the first quarter it was concluded that circuits with conductor widths down to .010" can be satisfactorily etched using either the spray or splash etching method if the artwork is compensated for the expected conductor width loss during the etching operation. It was also determined that this conductor width loss is approximately equivalent to the copper material thickness.

In the reported period, some additional tests were performed which were required to present a complete picture of thin conductor etching.

4.1.3 Effect of Fresh and Spent Baths on Conductor Loss

During the etching of large batches of panels, the etching solution slowly saturates with copper and its effectiveness gradually decreases. This saturation manifests itself in a longer etching period which might have some effect on conductor loss. The results given in Figure 4.4 and Table I below indicate that conductor loss is not affected by the condition of the bath.

TABLE I

Effect of New and Spent Bath on Conductor Width

ORIGINAL LINE WIDTH	COPPER THICKNESS	BATH CONDITION	AVERAGE CONDUCTOR WIDTH
.010"	.0028"	New	.00688
.010"	.0028"	Spent	.00708
.020"	.0028"	New	.01720
.020"	.0028"	Spent	.01705

The variations of the .010" conductors was about 3% and of the .020" conductors about 1%. This can be considered negligible. Only the spray etching technique has been used for determination of above results, since it had been previously selected as most efficient of the three etching methods investigated. The variations in time to etch through .0028" copper foil was: Fresh Solution - 2 1/2 minutes; Spent Solution - about 5 minutes.

4.1.4 Variation in Conductor Loss

The reproducibility of results from part to part and the uniformity of etching in different areas of the same pattern is of prime importance when working with thin conductors. Careful measurements of various areas of patterns were made and the results tabulated and compared with results obtained during previous tests.

It was found that within the same pattern, using .0028 thick copper, the conductor width variation from the expected width was $^{+2.2}_{-3.4}$% for spray etching and $^{+2.7}_{-6.5}$% for splash etching. The variation from the expected conductor width within groups of specimens was $^{+11.9}_{-13.1}$% for spray etching and $^{+11.3}_{-17.8}$% for splash etching. The larger variation of conductor width observed in splash etching is probably because the parts are not visible during the etching operation and slight overetching is possible. In spray etching, the parts can be observed through a window and the process can be stopped as soon as the etching is completed.

4.1.5 The Shape of the Undercut

In this report, as in the first report, the amount of conductor left after etching was measured at the top portion of the conductor. A careful investigation of the cross section of the etched conductor was made to determine how accurately this value represents the remaining cross sectional area of the conductor. Figure 4-5 and Photomicrograph 4-7 show cross sections of specimens etched by spray and splash etching methods. (Tank etching was not investigated since previous work indicated that this technique was not usable for fine conductor etching. See Quarterly Report #1).

It is evident that the conductor is wider at the bottom than at the top after spray etching by an average of 1.6 mils and after splash etching by about 2.0 mils (for .0028 thick copper foil).

From Figure 4-5 it is also evident that spray etching leaves no undercut whatsoever, i.e., the conductor cross section is a regular trapezoid with the wider portion on the bottom. The splash etching method produces a slight undercut at about 2/3 of the conductor height, but the average conductor width loss at the bottom is almost negligible: 0.7 mils compared to the 2.87 mils lost on the top.

The cross sections indicate that during the etching process, most material removal is occurring just below the etch resist film and that the thinnest portion of the etched conductor is near the top. All presented data is describing the worst case; the value of the maximal line loss.

The results also indicate that in areas of close conductor spacings, allowances should be made for the proper distances between conductors tc avoid possible voltage breakdowns. This is especially important to remember when the artwork is compensated for expected conductor loss on top. More detailed summaries of the results can be found in the last page of the complete data sheets of performed measurements given at the end of the report.

4.2 LAMINATION CYCLES

4.2.1 Background

In the Quarterly Report #1, the results of the investigation about the effects of a preheat or "gel" period (during which the semicured "B" expoxy is in the liquid state) have been reported. It was determined that the optimum duration of such a "gel" period is about 4 minutes. In the second quarter, the investigation of the cure cycle proper has been conducted.

4.2.2 Heat and Pressure Required During the Curing Process

The epoxy resins used for the preparation of laminates must be cured under simultaneous application of heat and pressure. In the manufacture of multilayers, a sheet of woven fiberglass impregnated with semicured epoxy is used as an adhesive between two layers of fully cured circuit layers. There are now a number of vendors which sell such "B" stage epoxy fiberglass sheets.

A number of samples of "B" stage material have been investigated but manufacturer specifications about storage, handling, and the recommended cure cycle for the respective materials vary significantly. Therefore, it is rather hard to prescribe a universal and uniform laminating cycle for all of the available materials. In all cases, when the manufacturers' instructions were followed, the final laminate was satisfactory in all respects.

Despite variations in detail, the specifications of all materials tested were within the following outline:

a. Storage: Room temperature, but as dry as possible (it has already been mentioned in Quarterly Report #1 that for the best results a controlled humidity room (40% R.H.) must be established and all prelaminating operations performed there).

b. Storage Life: Three to six months.

c. Preheat or Gel Period: within the limits reported in the Quarterly Report #1 (about 4± 1 minutes).

d. Laminating Temperature: 320 F. to 350 F.

e. Laminating Pressure: 100 to 1000 psi

f. Curing Time: 8 to 45 minutes

g. Cooling: Slow ambient air cooling is preferred, but water jacket cooling is satisfactory. Cooling should be done while the laminate is under full pressure.

During this investigation the following observations were made: If the temperature during the curing cycle is permitted to fall below 300 F., the curing will not be satisfactory and the board might blister during the soldering or heat cycling. The range of pressures which will make satisfactory laminated boards for all tested samples was rather wide and pressure selection is mostly dictated by the circuit geometry, overall thickness, and type of adhesive.

The curing time also has a wide range but since a longer curing cycle produces a more fully cured resin, it is suggested that the cycle time be greater than the lower limits of the specified range despite economic conditions, i.e., shorter press time. However, a too long curing cycle can "overcure" the resin which may then become brittle. When working within the time range specified by the manufacturer, satisfactory laminates were obtained. No discernible effects on the final board were observed when the speed of cooling after curing was varied.

4.2.3 Backing Materials

The customary practice for the laminating of sheet laminates is to cure the laminates directly against press platens. This produces uniform and flat laminates. In the case of multilayer boards, this technique also produces very flat, uniform surfaces on the laminated board. Since the multilayer board consists of a number of imbedded circuit layers, the pressure distribution within the board is not uniform, especially if there are identical circuit patterns superimposed one above another. At such high points the pressure is much higher than in areas where circuitry is etched away and almost all the adhesive is squeezed out. The low points receive insufficient pressure and do not laminate properly. Such unequal pressure distribution was clearly evident in the lamination of the dielectric (comb) test pattern for this contract.

To equalize the pressure distribution, a number of flat resilient materials have been investigated which were placed between the stacked circuit layers and the top and bottom plates of the laminating jig. Cork sheets could not withstand the temperature; Teflon and Silicone rubber sheets, .020" to .032" thick were very good. They produced good, uniform laminates and the adhesive flash did not stick to them. They are reusable, but a few hours must elapse between their use in order to give them time for springback and to remove the imprints of the pattern.

Further investigation was made using kraft paper with and without a layer of aluminum. It has been found that a stack of kraft paper .028" to .013" thick on each side of the board will give very good laminates. In order to prevent epoxy from adhering to the paper, a layer of .002" or .003" aluminum foil can be placed between the kraft paper and the circuit surfaces. However, when laminating multilayers with copper foil on both outside surfaces of the board, aluminum foil can be eliminated since copper will not stick to kraft paper. After trimming off flash, the paper is easily removed from the board.

From economic considerations, kraft paper is the most efficient material to use as a backing material. Kraft paper has a somewhat nonuniform texture which produces a copper surface on the laminated board which is not ideally flat. After the etching of copper from the surface (after drilling and plating) this nonuniformity of the surface is completely unobservable. This aspect of kraft paper is definitely not detrimental to the finished multilayer board and is mentioned only for reasons of completeness.

In all cases, when resilient "backing" layers were used during lamination, the surface of the laminated boards exhibited slight raisings at the points where the circuitry on the inner layers was repetitive.

4.2.4 Layer to Layer Registration

The exact registration of circuit patterns on different layers is of prime importance for the successful production of multilayer circuits. This problem is even more critical for production of microminiaturized circuits where layer to layer misregistration of more than $\pm$ .003" will seriously affect the reliability of the entire board because the drilled holes may miss the pad area and thus decrease the contact area between pad and plated through hole. Serious consideration was given to this problem and exact measurements of the amount of misregistration were made on numerous samples.

In the production of regular multilayer boards, special "bullseyes" are placed around the perimeter of the part during the artwork preparation. These bullseyes are registered on a coordinatograph with the circuit artwork within $\pm$ .002 max. variation before reduction and are repeated with the same accuracy on each layer of the board. After printing and etching of the layers, each of these holes is accurately drilled (within $\pm$ .002").

These holes are then used to pin each layer in the laminating jig within the required registration tolerance. On regular parts, these holes are spaced uniformly 5" to 6" apart around the entire perimeter.

The measurement of misregistration in these parts established that there was never more than $\pm$ .005" when this production technique was used. But, as mentioned above, for microminiature multilayer circuits a $\pm$ .003" tolerance must be held.

In order to achieve this registration, artwork has been prepared with the location of the bullseyes for the mounting holes within ± .001". Also, the mounting holes were spaced at closer intervals. As seen from Figure 4-8, the registration of all layers on such a part was held within ± .003" of the true location.

An investigation was then made to determine the maximum spacing of the mounting holes which would still provide registration of the layers within ± .003". It has been determined that with spacing up to 4" between mounting holes, such registration is possible.

All investigations, so far, indicate that when the mounting holes are spaced at the required intervals around the perimeter of the part, there is a negligible amount of shifting of the base material and circuitry during the lamination cycle.

4.2.5 Tooling for the Lamination Process

As is evident from paragraph 4.2.4, the exact location and immobility of each layer during the lamination cycle is a very important condition for the successful lamination of multilayer boards. To achieve this, each circuit layer must be firmly pinned down during the entire laminating cycle. For this purpose, special jigs are manufactured which consist of two flat plates in which holes for pins are drilled in exactly the same positions as are the "bullseyes" on each layer.

The requirements for these plates are quite stringent; they must:

1. remain perfectly flat through numerous heat and pressure cycles;

2. be thermally stable, i.e., the position of pins should not change appreciably when undergoing heating and cooling cycles, and;

3. be sufficiently hard so that no imprints or deformations of the surface are evident after prolonged use. Repeated insertion and removal of the pins should not damage or increase the diameter of the locating holes.

An investigation of the best materials for such plates was made. Aluminum jig plates were tried but it was found that this material is too soft to withstand the repeated pressure cycle and that after a period of time, a definite deformation is observed on the surface and in the location holes. Stainless steel plates have shown some thermal deformation - slight buckling - after repeated heat and pressure cycling. The material which has shown the best characteristics is ground steel stock. The desired thickness of this material for laminating plates is 3/8". This thickness is available in various lengths but only up to 10" in width. Because it can be purchased in larger sheets, 1/4" thick material was tested and found satisfactory for the larger boards. The pins used were 1/8" diameter. Usually, the perimeter of the laminating jig is 1/2" to 1" away from the center line of the locating holes.

4.3 SMALL HOLE DRILLING

4.3.1 The Objective

The object of this investigation is to determine production processes which will be adequate for drilling clean, very small diameter holes in multilayer circuit boards with minimum mis-registration between the hole and the circuit pattern.

4.3.2 Background

The drilling of holes in fiberglass reinforced epoxy copper clad laminates is quite a complicated process. In the drilling operation, the drill advances through layers of copper foil and epoxy-fiberglass material which have completely different machining characteristics. The base laminate material itself is not homogeneous since it consists of soft resinous epoxy and hard brittle fibers of glass. Glass fibers do not shear evenly and the holes drilled in such materials are irregular and have rough walls. Great care must be taken to have proper drilling conditions in order to minimize such irregularities and obtain good holes. When drilling holes in multilayer circuits, the situation is aggravated since the drills go through alternate layers of copper, semicured adhesive and fully cured base laminate layers. Such conditions impose even more stringent requirements and controls for small drilling in epoxy fiberglass multilayer boards.

4.3.3 Investigation of Drilling Conditions in Multilayer Boards.

For some time it has been known that non-homogeneous materials, as found in multilayered boards, introduce conditions not found when drilling regular two-sided boards. The ratio of board thickness to the hole diameter is usually larger in multilayer boards. Also the heat generation during the drilling causes a thin layer of epoxy on the periphery of the hole to become plastic. The epoxy fills the flutes of the drill and hardens, preventing the removal of chips which causes even greater heat. Occasionally, a thin layer of resin is deposited over the exposed copper of the pads on the inner layers. If this occurs, there will be no electrical connection between the pads on the inner layers and the plated-through hole. Figure 4-9 shows such a smear.

A thorough investigation of the conditions which lead to such smear formation was made. After numerous tests, it was evident that all factors and variables which can be present during the drilling process require tight controls because each single factor, if it is left uncontrolled, can contribute to the smear formation.

These factors are:

a. Drill conditions: drills must be sharp and therefore a change of drills after drilling 200 to 250 holes is mandatory. They must be properly sharpened so that the drill point is not off center. This causes accelerated wear and an oversized hole.

b. The material thickness should be limited, i.e., no panel stacking is possible. The drilled hole diameter should never be less than 30% of the overall material thickness.

c. Material should be sufficiently cured.

d. Drill speed and feed rates must be fixed for a given hole size.

4.3.4 Investigation of Drilling Speed and Feed Rates

For this investigation the following machines have been used: Photocircuits Corporation multiple spindle machines with fixed and variable speed heads, Zagar multispindle machine, Bridgeport milling machine, and Manex milling machine. The parts used were 6 to 8 layer multilayer boards. All drills were sharpened and inspected prior to testing. The speeds used were 1115 to 5700 rpm and feed rates were .0015 to .019 in/rev. Regular drills of various sizes were used.

The determination of hole condition was made by microsectioning techniques. An "Excellent" hole was a straight one with no smearing of epoxy. A "Good" hole was straight with no smears on the exposed copper but some smearing on the epoxy portion of the wall. A "Fair" hole was a straight one with some smearing on the copper but never on both sides of the copper and not through the entire cross section. A "Poor" hole was when excessive smearing over the exposed copper was observed, the copper pads showed bad burrs and/or the hole was not straight.

The results of this observation indicate that for holes drilled with a #60 drill or larger, the speed of drilling must be controlled to have about 35 surface feet/min. peripheral speed and a feed rate of .0045"/revolution. For smaller holes, the peripheral speed should be about 20 SFM and the feed rate .003"/revolution. Photomicrographs #4-10 and 4-11 show a hole with an excellent pad-to-hole connection.

4.3.5 Tooling for Small Hole Drilling

One requirement which is very critical for drilling holes in miniaturized circuits is a minimum of misregistration between the hole and the pads on the inner layers. Since all circuit layers are encapsulated, there cannot be any adjustment of circuit patterns to the drill pattern as is possible with regular two-sided boards with plated-through holes. In the case of the multilayer circuit, the pattern of the holes must be exactly positioned over the circuit pattern and each hole must be drilled within $\pm$ .002" of the encapsulated circuit pad. Such stringent requirements led to a reevaluation of drilling techniques and the tooling presently used for regular printed circuit manufacture.

The mounting holes used for the registry and mounting of individual layers on the pins of the laminating jigs can serve as efficient guides for registering the laminated part on the drill table (for the automatic multispindle machines) or in the drill jig. The maximum misregistration of each individual mounting hole is $\pm$ .002" (see Section 4.3) and this tolerance is adequate for the registering of the drill pattern to the circuit pattern in microminiaturized multilayers.

The drilling of individual holes presented a more difficult problem. The drills used for drilling miniaturized holes are very thin, flexible, and rather weak. In order to place the holes with the required accuracy, the drill and its travel must be short and it should be positioned with a bushing or a very accurate drill jig. Also, for best results, a sequence of a repetitive lifting of the drill (pecking motion) from the hole during drilling is desirable to facilitate chip removal. If this is not done, the unremoved material clogs the drills which results in frequent and excessive drill breakage.

The use of drill jigs could remove some of the above obstacles but sound production practice required such jigs be made of hardened and fairly thick tool steel. Hardening after fabrication could not be used because this produces dimensional changes larger than are permitted by the requirements. In addition, the drilling of such small holes in 1/4" or 3/16" thick steel, produced jigs which had on the bottom (i.e., on the surface which will be against the part) a misregistration between isolated holes of more than .003" because of drill travel from the vertical during the fabrication of the jig.

The solution to the tooling problem was found in the use of "upside down" drilling machines. In such machines, a conical stylus is pressing onto a drill jig which has only countersunk centers on the surface at the location of each hole. When the jig is centered and clamped by the stylus the drill advances from underneath and drills holes in the circuit boards which are positioned under the drill jig. The travel height of the drill is controlled so that it drills through the boards into backup boards of scrap material and not into the jig. With such a technique there was no need to manufacture deep holes in the drill jig; only countersinking with a center drill to produce an accurate jig. A number of miniaturized multilayer parts have been manufactured and they demonstrated the required hole location tolerances when this "upside down" system was used for the drilling of holes.

These machines have variable speed spindles, variable feeds, and normally use carbide drills. The machine provides a very strong clamping action which holds the parts steady and is one of the keys to good drilling. There is no "pecking" motion but the upside down drilling provides a gravity assist for chip removal. An air stream is also used to facilitate chip removal. Investigation of the holes after they are drilled on "upside down" machines showed that these holes were excellent. They were straight and no evidence of smears was observed when proper feed and speed rates were used.

4.4 MICROMINIATURE PLATED-THROUGH HOLES

4.4.1 Objective

The objective of this investigation was to determine the parameters for a reliable microminiature plated-through hole using regular production methods.

4.4.2 Background

In order to achieve the degree of miniaturization required for the interconnection of modules with very closely spaced pins, multilayer circuits must have very small plated-through holes. The after plating diameter of such holes should be about .020". Since the overall board thickness is close to 1/16", such holes are beyond the capability of conventional printed circuit technology. The technique for the production of plated-through holes is well established, but as a rule of thumb, regular printed circuits have hole diameters no less than 2/3 of the overall thickness. In very small holes a problem arises with the efficiency of metal deposition into the hole, i.e., at an angle to the direction of the major ionic flow. The term "throwing power" has been used in plating technology to describe the ability of a given plating bath to deposit the metal in areas which are not perpendicular to the ionic current. Therefore, for the plating of small holes in relatively thick material, all baths with poor throwing power, such as acid copper, are excluded. The use of copper baths with improved throwing power, such as copper pyrophosphate or copper cyanide, was precluded for a number of years because no plating resist inks for these baths were available. Presently, a number of satisfactory inks for a copper pyrophosphate bath can be purchased and this bath has been used exclusively for the investigation of small hole plating.

4.4.3 Hole Diameter to the Material Thickness Ratio

As mentioned above, the production of reliable microminiature plated-through holes hinges on the ability to deposit sufficient metal into a narrow, long drilled hole.

In order to evaluate this ability, a test was performed using 5 layer multilayer boards with an overall thickness of .062". In these boards, a large number of holes of varying diameter were drilled. After adherent copper reduction, the boards were panel plated in a pyrophosphate bath. The term "panel plating" denotes plating of the whole surface of the circuit panel and is contrasted to the term "pattern plating" where only the required circuit pattern is plated and other areas are masked off by a plating resist ink. Table II shows the results.

TABLE II

Results of Panel Plating of Very Small Holes

Drilled Hole Dia. (mils)	Material Thickness Hole Dia. Ratio	Min. Plating on the hole wall (mils)	Plating in the Hole to the surface ratio
22.5	2.75	.86	1:1.38
21.1	2.95	.81	1:1.45
17.0	3.65	.89	1:1.33
15.0	4.15	.80	1:1.53
14.0	4.4	.88	1:1.35

These results indicate that a small hole with a diameter smaller than 25% of the material thickness can be satisfactorily panel-plated when using a pyrophosphate copper bath. It is interesting that the plating thickness in the hole did not show any appreciable difference with a decrease of the diameter nor did the plating throwing power change with variation in diameter. (The last column is a relative measure of the throwing power. A bath with poor throwing power will have a much higher ratio about 1:3 or thereabouts).

Figures 4-12 and 4-13 show some photomicrographs made from the holes of this test. From these photographs, it is clearly visible how uniform the plating is throughout the length of the hole. Also, note that the top and bottom surfaces of the board still have a .0028" thick layer of copper foil. The copper plating deposit is above the faintly visible demarcation line and its thickness is only slightly more than the thickness of the copper deposit in the hole. A very similar appearance is visible in photomicrograph 4-14 which has a .028" hole drilled in .102 material (3.65 ratio).

4.4.4 Pattern Plating of Small Holes

On conventional two-sided printed circuits with plated-through holes, the circuit patterns are screened after hole metalizing and the holes and the pattern are plated simultaneously. With ultraminiature multilayers with holes spaced at .075" intervals, all circuit patterns must be encapsulated on internal layers and no circuits are possible on the surface because of tight dimensional requirements. Therefore, only the holes and their surrounding pads are plated in the plating operation. In microminiature multilayers, where hole spacing is down to .050", there is no room on the surface even for pads around the holes and such circuits must have "landless" holes. For "landless" holes the pattern applied to microminiaturized circuits is essentially a continuous plating mask and metal is deposited only in the stem of the holes. During plating, a certain amount of metal is deposited on the surface of the board forming a metallic annular ring around the periphery of the hole.

During such plating, the field and current distribution is completely different from the distribution during panel plating. The area of highest current density is at the orifices of the holes and there most of the metal is deposited at this point. To test this distribution, a number of samples .102" thick were drilled with .025" diameter holes (4:1 ratio) and their surface was completely masked with ink after copper reduction. These samples were then plated in a conventional pyrophosphate plating tank. Photomicrograph 4-15 shows the results of this plating. Despite the fairly uniform wall plating of .002" inside the hole, a tremendous plating buildup is observed at the edge of the hole. Measurements of a number of these nodules at the orifices of the holes were as follows:

Thickness of the copper at the orifices: .0047" to .0060"
Max. heights of the buildup above the foil: .006" to .0136"
Extension of the buildup beyond the edge of the hole: .010" to .013"

It is evident that this plating buildup makes it useless to use hole gauges for hole diameter determinations. Also, the buildup on the surface may short closely spaced holes. The wide variation observed in the measurements of these nodules indicates that their formation is nonuniform and would be very hard to control. Some additional tests were run with similar hole parameters.

These tests again exhibited a plating buildup which was 2.5 times greater at the edge of the hole and 3.2 times greater on the surface when compared to the plating in the center of the hole. In the board with a smaller hole to material thickness ratio (.070 material with .025 hole diameter) this buildup decreased to approximately 1.5 to 1.6 times the plating thickness in the hole.

4.4.5 Plating of Etch Resistant Metal

After the initial copper deposit is plated into the hole to the required thickness, an etch resistant metal must be plated over the copper to protect the holes when the unwanted copper foil is etched away from the surfaces of the board. Etch resistant metals widely used in industry are solder and gold. From an economy standpoint, solder is preferred since it is considerably cheaper than gold. Figure 4-16 shows the results of solder plating a microminiaturized (.025" diameter) hole. As can be seen from the photomicrograph, there is a very strong buildup of solder at the orifices of the hole and a negligible thickness of solder deposit inside the hole. Solder plating baths have poor throwing power which explains the observed results. This poor throwing power definitely precludes the use of solder plate as an etch resist for miniaturized holes.

NOTE that in photomicrograph 4-16 one pad is not connected to the plated through hole because the test pattern included an etched hole center in the pad.

Gold has much better throwing power than solder. However, it was found that solderability of printed circuit boards with gold plated holes is significantly improved by plating a nickel layer under the gold. Nickel has very good throwing power and also exhibits a leveling effect, i.e., it will plate inside of any irregularities which have been produced during copper plating. After filling crevices and irregularities, the nickel will keep depositing a fairly even and uniform plating which smooths out the hole walls. Plated nickel is strong structurally and gives added strength to the copper plating in the hole, thus making the plated-through hole much tougher. All available data on past performance of multilayer circuits indicates the superiority of the copper, nickel, gold plated-through holes. Since solder plating cannot be used in microminiaturized holes and since the use of nickel and gold over copper offers definite advantages, such a plating system has been selected for this study.

4.4.6 Plating of Small Holes

It has been determined in the above described investigation that the best uniformity of copper plating in the holes was obtained when circuits with microminiaturized holes were panel-plated. In this case, copper plating is deposited on the surface of the board over the existing foil. This leaves a fairly thick layer of copper on the surface which has to be etched away after the etch resistant material has been plated in the holes. The etching time is long and produces a severe undercut at the orifice of the holes. The undercut might, in certain cases, completely remove the plating overhang of the "landless" plated-through hole and even etch a few mils into the stem of the hole as is shown in Figure 4-17.

The screening of plating mask on the surface of boards with very small holes also presents some difficulty. In some cases the ink will deposit a continuous film over the hole or, in other cases, will seep into the hole. In both instances, additional cleaning operations are required to insure continuous plating inside the holes.

It is also a problem to determine the proper current density when plating parts which have no circuit pattern on the surface because the plating area is limited to just the holes. This control can be achieved either by control over the voltage of the plating tank or by control of the current supplied to the tank. For plating microminiature holes, a number of tests have been run to determine the feasibility of using the voltage control method as a guide for the proper current density. This method can be fairly efficient when panel plating is employed. In such cases, when the plating area is changed, the current will change proportionally at the same voltage setting, keeping the current density almost constant. However, the voltage control method is not accurate when circuit pattern plating is used and as the results below show, it is a completely unsatisfactory method when plating landless holes with surface of the board completely masked.

The total plating area inside the holes was .0294 sq. ft. At 1.77 volts the recorded amperage was 14.4 amps making a plating current density of 153 amps per sq. ft. A completely identical board having an overall thickness of .030" was used in a second test. The actual plating area in the second board was exactly half that of the first board. At 1.76 volts the plating current was 13.6 amps, i.e., it did not decrease proportionally to the area. For the second board, the current density was about 290 amps per sq. ft. which is excessively high.

The above discussion indicates that the plating of microminiature landless holes is a difficult process and work is under way to determine the best process for obtaining uniform and reliable holes with a minimum of plating buildup around the edge of the hole.

SECTION 5

CONCLUSIONS

1. There was no significant difference observed in conductor width loss when etched in either a newly mixed or an almost completely spent spray etching solution. The time of etching through a given foil thickness, naturally, increases gradually with the use of the bath, and for optimum results, the operator must constantly observe the etching process and stop it as soon as complete etching is observed.

2. A variation in conductor loss of $^{+2.2}_{-3.4}$% from expected width was observed within the same specimen and $^{+11.9}_{-13.1}$% variation in different batches of specimens after spray etching. In splash etching, this variation was somewhat greater. This observation effectively sets the limits for conductor width tolerances which can be held in thin conductor etching.

3. The shape of the conductor cross section after spray etching is a trapezoid with the wider base at the bottom of the conductor, i.e., the maximum conductor loss occurs just below the etch resist film. When the artwork is compensated for the expected line loss on the top of conductors, a careful account of the larger conductor width at the bottom must be made in order not to jeopardize the minimum spacing requirements.

4. The lamination cycle parameters such as: temperature, pressure and cure time, depend largely on the type of "B" stage semi-cured resin used for lamination. In all cases, when the manufacturers' instructions were followed, a good laminate resulted. Generally, these parameters can be varied within certain ranges without detrimental effect on the subsequent performance of the laminate.

5. In order to equalize the pressure distribution within a multilayered stack of circuits during the lamination operation, a resilient "backing" layer must be placed between the circuit layup and the laminating jig plates. Teflon, silicone rubber, or kraft paper sheets can be effectively used for this purpose.

6. All layers must be immobilized during the lamination operation to preserve the proper layer to layer registration. To accomplish this, each layer must have special mounting holes around the periphery of the part for pinning in special jigs during lamination. For a maximum of $\pm$ .003" misregistration from layer to layer (noncumulative) these mounting holes must be no more than 4" apart.

7. For the manufacture of laminating jigs, only 1/4" or thicker ground steel plates should be used because of their dimensional stability under repetitive heat and pressure cycling.

8. All variables of the drilling operation must be carefully controlled when holes are drilled in multilayer printed circuit boards. Under uncontrolled conditions, a combination of factors can arise which will lead to the formation of plastic smears over the exposed copper inside the hole and thus produce electrical discontinuity between the circuit layers and the plated-through hole.

9. For best results, drill speed and feed rates must be fixed for given sizes of holes in multilayer boards.

10. Tight tolerances for hole locations on microminiature multilayer boards and small gauge drills prevent the use of conventional drilling methods and tooling. The required accuracy of drilling was obtained when an upside down drilling method with special templates and carbide drills were used.

11. In order to obtain small diameter plated-through holes in thick laminates, only plating baths with high "throwing power" should be used. When panel plating multilayer boards in a copper pyrophosphate bath, holes down to .013" in diameter were successfully plated in .062 thick material. This indicates the possibility of obtaining multilayer holes with diameters about 25% of the overall material thickness.

12. Conventional plating techniques are evidently inadequate to produce good, small, deep, holes when plating only "landless" holes; i.e., when the whole surface of the board is completely masked off. Under such conditions, a very nonuniform plating inside the hole is observed because of heavier plating buildup at the orifice of the hole.

13. Poor throwing power precludes the use of solder plate as an etch resist for miniaturized "landless" plated-through holes. A nickel-gold combination produces good results and shows uniform plating throughout the hole.

14. Further investigation of production techniques for the manufacture of reliable, small "landless" holes is required.

SECTION 6

PROGRAM FOR NEXT INTERVAL

During the third quarter of the subject contract, the following work will be performed:

1. Further investigation for the fabrication of microminiaturized layered printed wiring will be carried out in the areas of:

   a. Small hole cleaning.

   b. Small hole plating and etching techniques.

2. Processes will be standardized and a production specification for the fabrication of test samples will be issued.

3. An In-process Quality Assurance system will be established.

4. Quality Control procedures and detailed testing schedules for sample inspection and testing will be prepared.

5. Tooling for the production of microminiaturized printed wiring samples will be designed and fabricated.

6. Required types and quantities of samples will be manufactured.

SECTION 7

IDENTIFICATION OF KEY TECHNICAL PERSONNEL

During the second quarter the following persons took part in the work covered by this report:

TABLE 7 - 1

KEY TECHNICAL PERSONNEL

NAME	TITLE	MAN HOURS WORKED
G. Messner	Project Manager	133
R. McCaw	Senior Engineer	172
M. Paluszek	Production Engineer	337
F. W. Schneble	Director of Research	80
L. A. Gunsaulus	Quality Assurance Manager	33
----------	Technicians	717
----------	Shop labor	180

No new personnel have been added to the program during the reported period.

SECTION 8

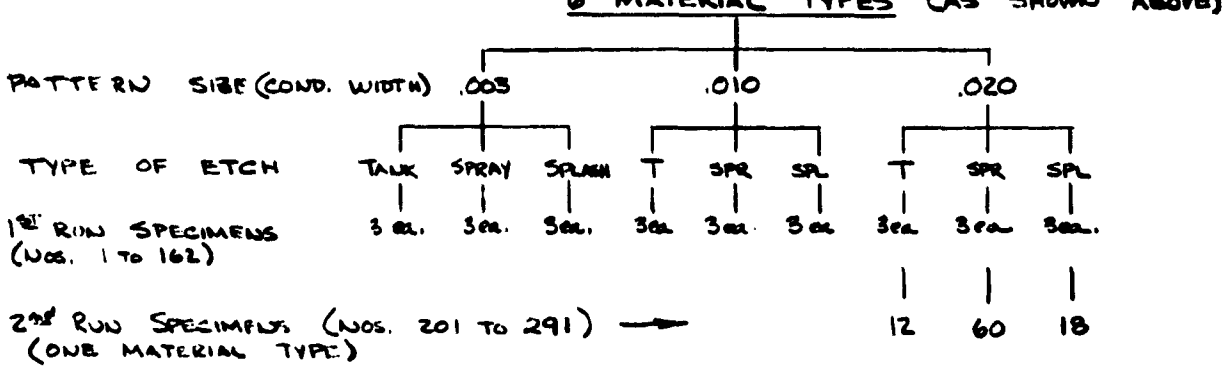
REFERENCES

BY_____ DATE_____ SUBJECT FINE LINE ETCHING SHEET NO. 1 OF 5

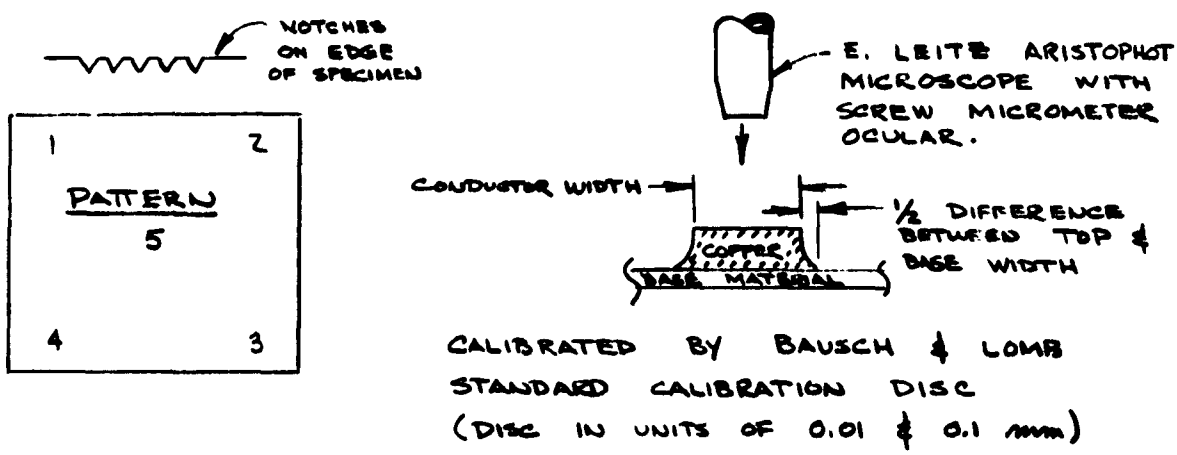
CHKD. BY KW DATE 12/14 JOB NO. 898

MATERIAL DESCRIPTION		ETCHING TIMES			IDENTIFICATION
Cu THICK. (Oz - IN.)	BASE THICK. (INCHES)	TANK (MIN)	SPRAY (MIN)	SPLASH (MIN)	NOTCHES OR NUMBERS
1 - .0014	.001	APPROX.	0:55	2:30	0 (1 TO 162)
2 - .0028	.001	10	1:35	5:00	1
2 - .0023	.002	↓	1:35	6:00	2
2 - .0028	.003	↓	1:35	5:30	3
½ - .0007	.008	↓	0:30	1:25	4
1 - .0014	.008	↓	0:55	2:45	6
2 - .0028	.008	12	2:00 TO 5:00	5:30	201 TO 291

LAYOUT OF TEST SPECIMENS



POSITION AND METHOD OF MEASUREMENTS

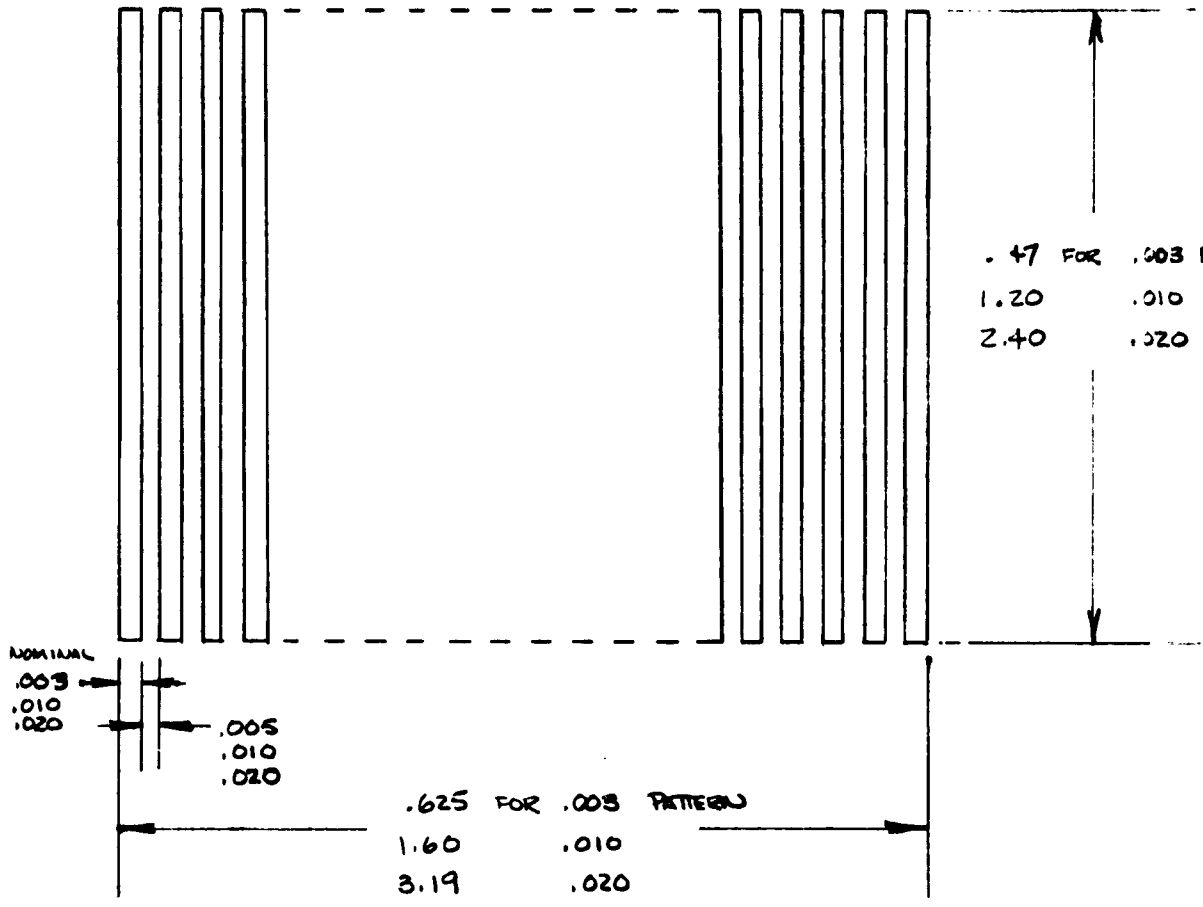


DESCRIPTION OF SPECIMENS, ETCHING TIMES, AND MEASUREMENT

THIN CONDUCTOR ETCHING Fig-4-1

BY L.S DATE 10/3 SUBJECT FINE LINE ETCHING SHEET NO. 2 OF 5
CHKD. BY [illegible] DATE 10-9 GLASSWORK JOB NO. 848

PATTERN OF EQUAL CONDUCTORS & SPACES



ALL GLASSES WERE MADE FROM SAME MASTER. ACTUAL DIMENSIONS OF LINES ARE GIVEN BELOW:

GLASS PATTERN	ACTUAL MEASUREMENTS (MICROSCOPE DIVISIONS) Position 1	2	3	4	5	AVERAGE (DIVISIONS)	CALIBRATION (INCHES/DIV.)	AVERAGE (INCHES)
.003	384	392	401	392	406	395	7.6×10^{-4}	.003
.010	697	678	685	701	693	690.7	15.15×10^{-4}	.01046
.020	664	680	686	678	694	680.4	30.6×10^{-4}	.02081

CONDUCTOR ETCHING GLASSWORK DATA FIG. 4-2

BY_____ DATE_____ SUBJECT FINE LINE ETCHING SHEET NO. 3 OF 5

CHKD. BY RCM DATE 12/14 JOB NO. 898

RESULTS

COPPER THICK (IN.)	PATTERN SIZE	LINE LOSS AFTER ETCHING (INCHES) TANK		SPRAY		SPLASH	
.0007	.003	NO PATTERN	.00406 AVE.	.00050	.00067 AVE.	.00038	.00048 AVE.
	.010	NO PATTERN		.00075		.00054	
	.020	.00406		.00076		.00051	
.0014	.003	NO PATTERN	.00518 AVE.	.00141	.00142 AVE.	.00118	.00116 AVE.
	.010	.00576		.00131		.00104	
	.020	.00421		.00156		.00126	
.0028	.003	NO PATTERN	.00429 AVE.	NO PATTERN	.00358 AVE.	.00172	.00287 AVE.
	.010	.00402		.00339		.00302	
	.020	.00451		.00372		.00322	

CU THICK (IN.)	PATTERN SIZE	ETCH PROCESS	TOTAL OF ALL MEASUREMENTS (MICROSCOPE DIV.)	# READINGS	AVERAGE WIDTH (DIV.)	CALIBRATION FACTOR (IN./DIV)	LINE WIDTH (IN.)	GLASS LINE WIDTH (IN.)	LINE LOSS (IN.)
.0007	.003	SPRAY	1045.8	15	69.7	3.59×10^{-5}	.00250	.00300	.00050
		SPLASH	1094.0	15	73.0	3.59×10^{-5}	.00262		.00038
.0014		SPRAY	1106.4	25	44.3	3.59×10^{-5}	.00159		.00141
		SPLASH	1266.4	25	50.8	3.59×10^{-5}	.00182		.00118
.0028		SPLASH	3075.0	15	205.0	7.68×10^{-6}	.00156		.00172
		SPLASH	415.2	15	27.7	3.59×10^{-5}	.00800		
.0007	.010	TANK	1967.4	15	131.0	3.73×10^{-5}	.00489	.01046	.00557
		SPRAY	3904.4	15	261.0	3.73×10^{-5}	.00971		.00075
		SPLASH	2667.2	10	266.7	3.73×10^{-5}	.00992		.00054
.0014		TANK	3774.0	30	125.8	3.73×10^{-5}	.00470		.00576
		SPRAY	7354.8	30	245.2	3.73×10^{-5}	.00915		.00131
		SPLASH	7584.1	30	252.8	3.73×10^{-5}	.00942		.00104
.0028		TANK	6032.2	35	173.5	3.73×10^{-5}	.00647		.00402
		TANK	10077	12	838.1	7.68×10^{-6}	.00642		

THIN CONDUCTOR ETCHING RESULTS Fig 4-3

BY_____ DATE_____ SUBJECT FINE LINE ETCHING SHEET NO. 4 OF 5

CHKD. BY RM DATE 12/14 JOB NO. 898

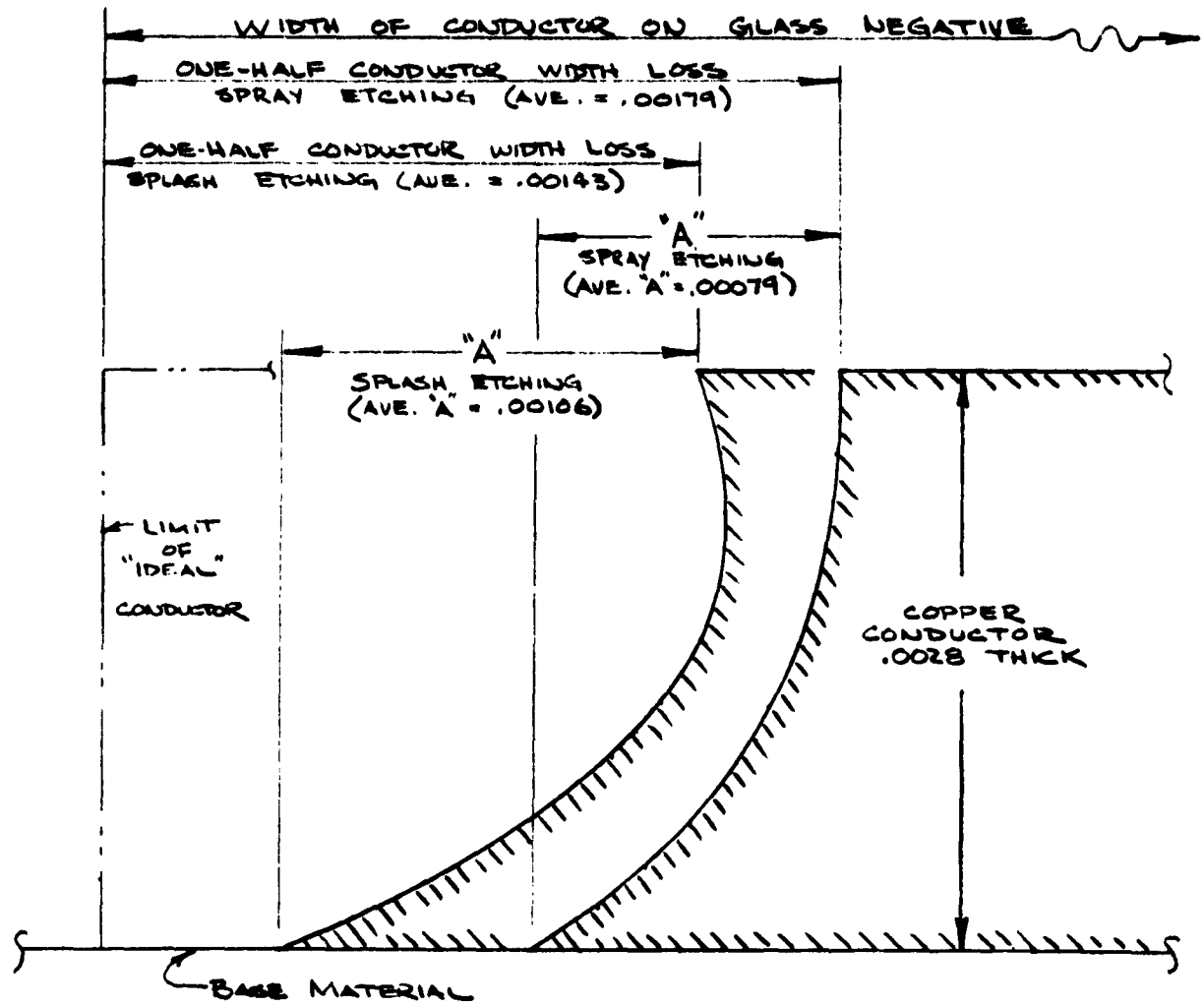
RESULTS

CU THICK (IN)	PATTERN SIBE	ETCH PROCESS	TOTAL OF ALL MEASUREMENTS (MICROSCOPE DIV)	# READING	AVERAGE WIDTH (DIV.)	CALIBRATION FACTOR (IN/DIV)	LINE WIDTH (IN)	GLASS LINE WIDTH (IN)	LINE LOSS (IN)
.0028 (CONT'D)	.010 (CONT'D)	SPRAY	8732.4	45	194.0	3.73×10^{-5}	.00725	.01046 (CONT'D)	
		SPRAY	8159.0	18	458.3	15.26×10^{-6}	.00692		
		SPENT BATH	27634.0	30	921.1	7.68×10^{-6}	.00708		.00339
		FRESH BATH	26,800.0	30	893.3	7.68×10^{-6}	.00688		
		SPLASH	8898.1	45	197.8	3.73×10^{-5}	.00738		.00302
		SPLASH	8979.0	18	498.3	15.26×10^{-6}	.00762		
.0007	.020	TANK	6678.0	15	445.0	3.77×10^{-5}	.01675	.02081	.00406
		SPRAY	8011.2	15	534.0		.02015		.00076
		SPLASH	8008.1	15	538.0		.02030		.00051
.0014		TANK	13186	30	439.5		.01660		.00421
		SPRAY	15349.2	30	511.6		.01925		.00156
		SPLASH	15532.6	30	517.8		.01955		.00126
.0028		TANK	19238.9	45	427.5		.01611		.00451
		TANK	21902.0	20	1095.1	15.26×10^{-6}	.01673		
		SPRAY	20576.6	45	458.1	3.77×10^{-5}	.01724		
		SPRAY	27326.0	25	1093.0	15.26×10^{-6}	.01670		.00372
		SPENT BATH	55,985.0	50	1119.7		.01705		
		FRESH BATH	56,205.0	50	1124.1		.01720		
		SPLASH	20785.4	45	463	3.77×10^{-5}	.01742		.00322
		SPLASH	34932.0	30	1164.4	15.26×10^{-6}	.01785		

THIN CONDUCTOR ETCHING RESULTS Fig 4-4

BY_____ DATE_____ SUBJECT FINE LINE ETCHING SHEET NO. 5 OF 5

CHKD. BY [illegible] DATE 6/14 JOB NO. 898



"A" = ONE-HALF DIFFERENCE BETWEEN TOP AND BASE CONDUCTOR WIDTHS

Cu THICK (IN.)	PATTERN SIZE	ETCH TYPE	TOTAL OF ALL READINGS (MICROM. DIVISIONS)	NUMBER OF READINGS	"A" AVERAGE (DIV.)	CALIBRATION FACTOR (IN./DIV.)	"A" AVERAGE (INCHES)
.0007	.010	SPRAY	1001.0	20	50.05	3.06×10^{-6}	.00015
.0007	.020	SPRAY	1192.0	20	59.60	↓	.00018
.0028	.010	SPLASH	6978.0	20	348.90	↓	.00106
.0028	.020	SPRAY	5141.0	20	257.05	↓	.00079

TYPICAL SECTION OF PRINT AND ETCH CONDUCTOR

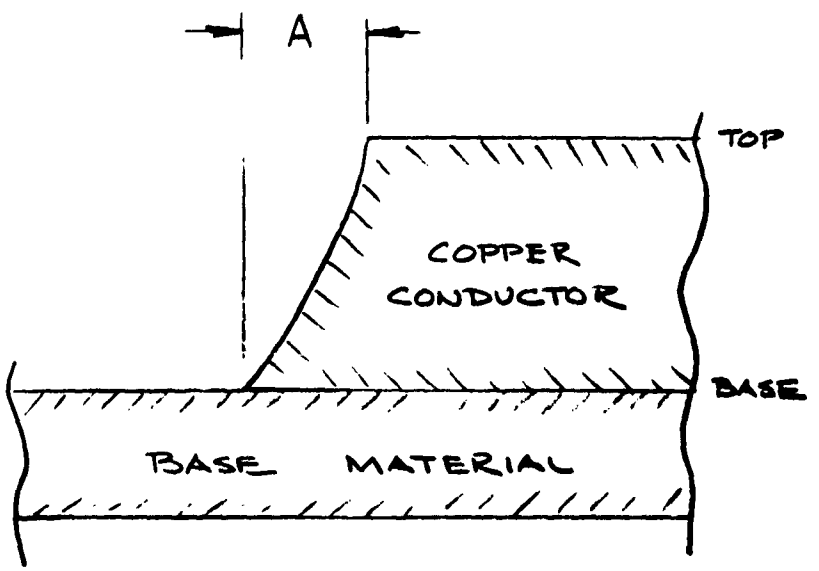
FIG. 4.5

BY_____ DATE_____ SUBJECT FINE LINE ETCHING SHEET NO. 8 OF 8

CHKD. BY KM DATE 12/13 JOB NO. 898

DATA SHEET

CU THICK (IN)	PATTERN SIZE	ETCH TYPE	"A" DIMENSION (½ DIFF BETWEEN TOP & BASE OF LINE) (MICROMETER DIVISIONS)					CALIBRATION FACTOR (IN/DIV)
.0028	.010	SPLASH	345	335	407	363	283	3.06×10^{-6}
			361	442	404	393	417	
			338	322	292	253	285	
			383	387	340	276	404	
.0028	.020	SPRAY	230	184	196	202	151	
			284	375	312	330	182	
			216	162	166	292	312	
			287	295	368	359	338	
.0007	.010	SPRAY	54	60	46	55	51	
			61	65	53	41	46	
			49	41	49	54	38	
			60	63	35	45	35	
.0007	.020	SPRAY	88	61	44	62	64	
			85	70	38	76	67	
			55	33	46	49	59	
			59	61	40	72	68	



STUDY OF SHAPE OF PRINT & ETCH LINE

Fig. 4-6

FIGURE 4 .7 Cross section of .0028" thick conductors after spray etching. Approximate magnification 180X.

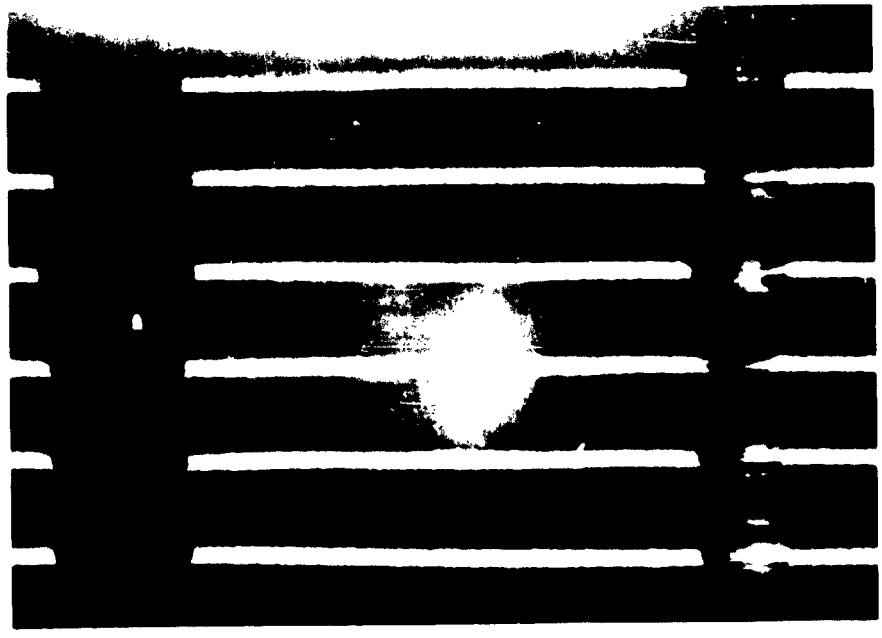


FIGURE 4.8 Cross section of a six layer circuit showing layer to layer registration. Approximate magnification 50X.

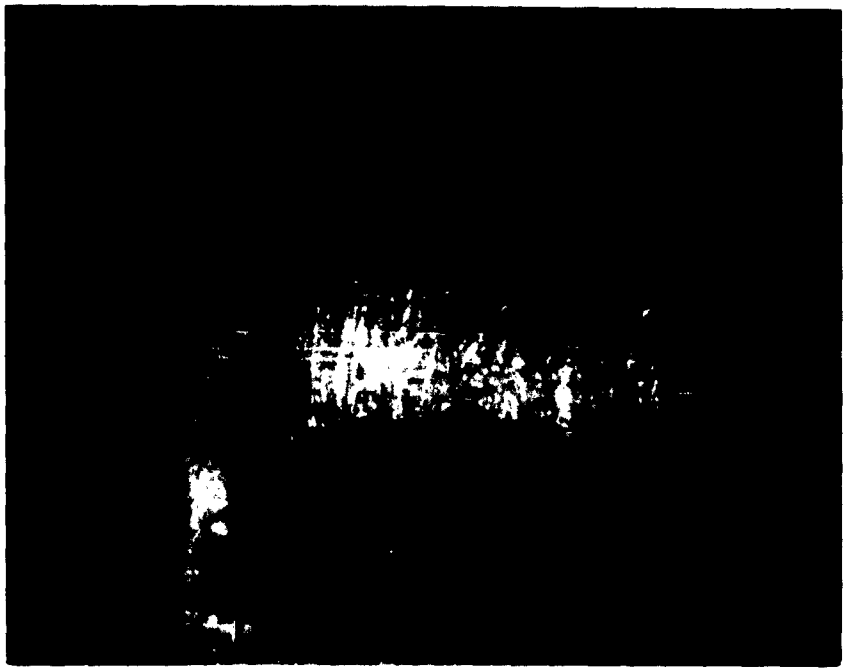


FIGURE 4.9 Plastic smear at the interconnection between the hole wall and an internal pad. Approximate magnification 350X.

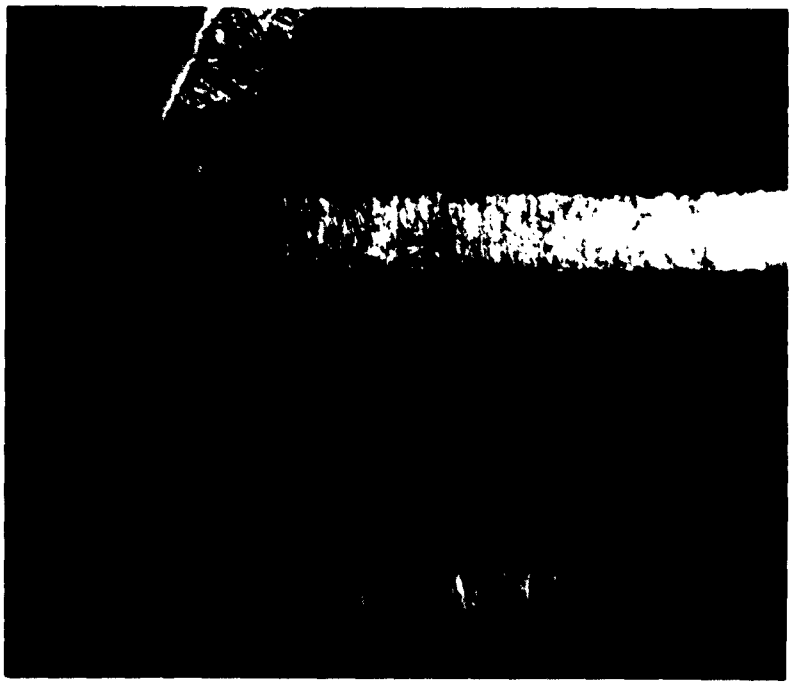


FIGURE 4.10 Proper interconnections between the hole and the internal pad. Approximate magnification 200X.

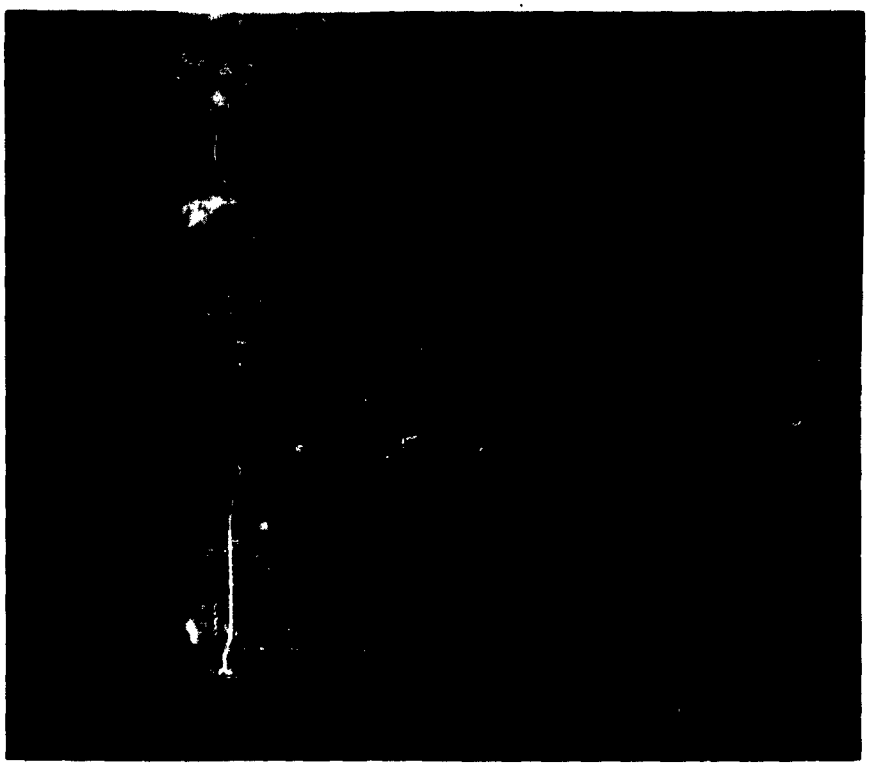


FIGURE 4.11 Proper interconnection between the hole and the internal pad. Approximate magnification 550X.

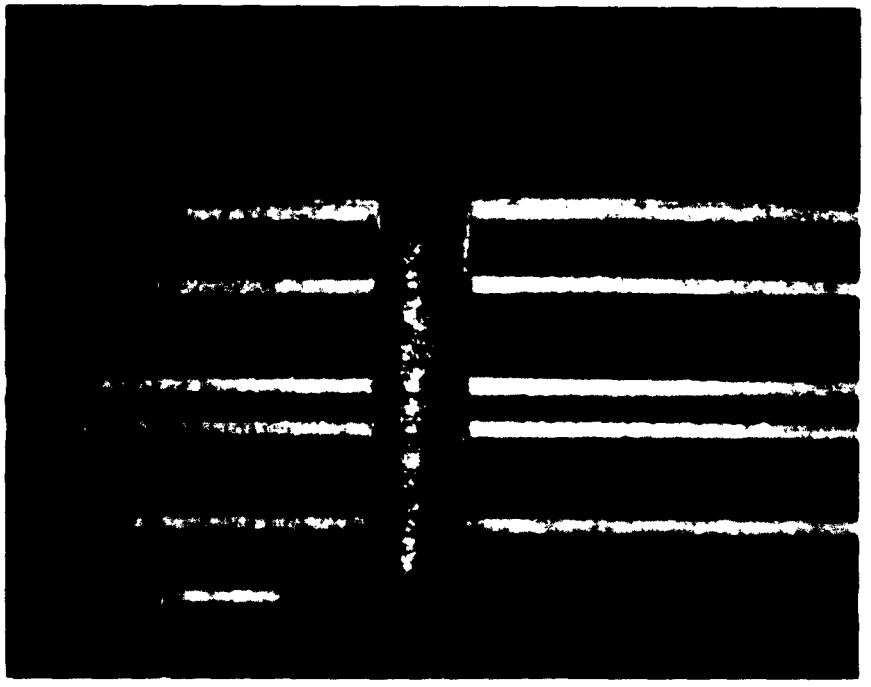


FIGURE 4.12 Cross section of a .014" diameter hole in a .062" multilayer. Approximate magnification 35X.

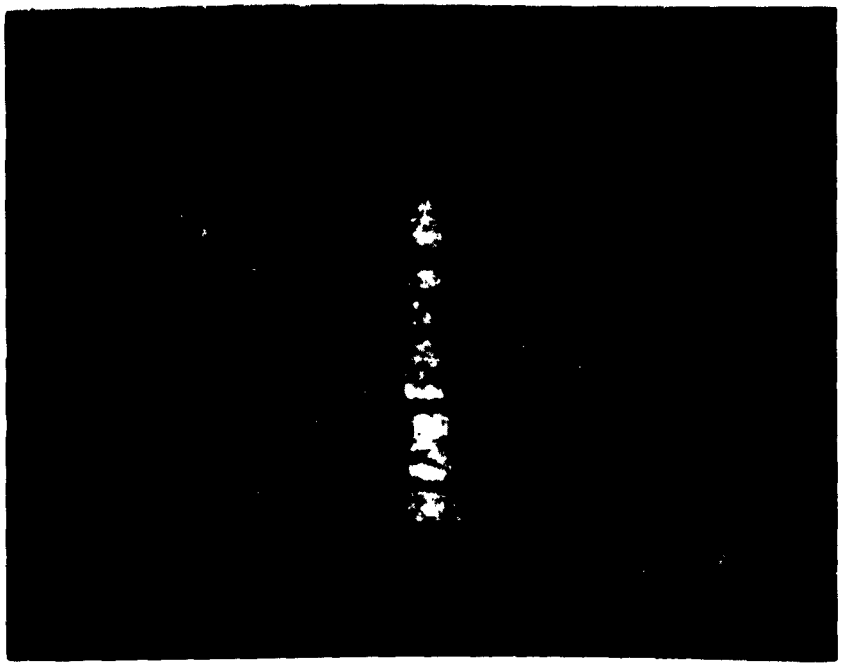


FIGURE 4.13 Cross section of a .025" hole in a .062" multilayer. Approximate magnification 45X.

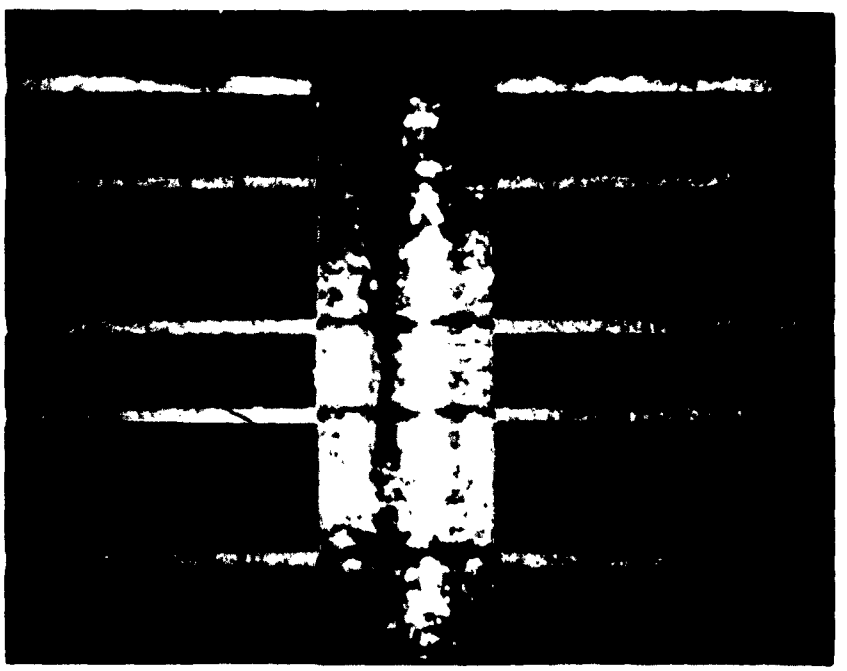


FIGURE 4.14 Cross section of a .030" diameter hole in a .102" multilayer. Approximate magnification 30X.

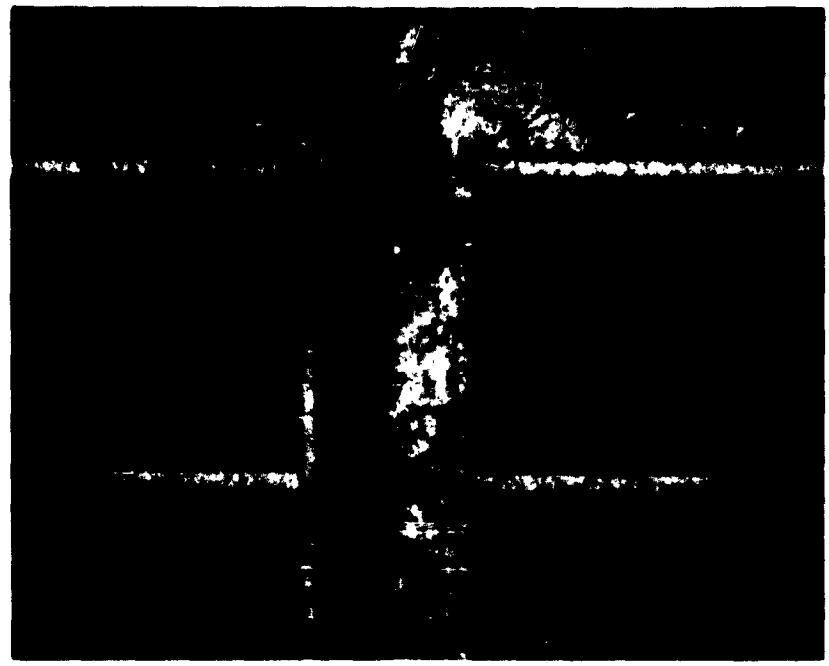


FIGURE 4.15 Copper plating buildup at the orifice of a .025" diameter hole.

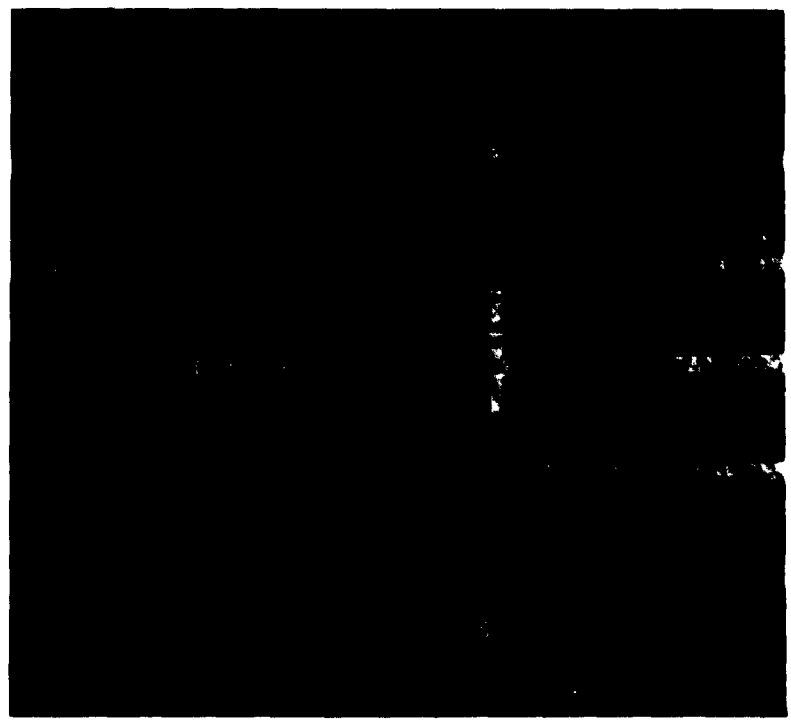


FIGURE 4.16 Solder plating over copper in small holes.

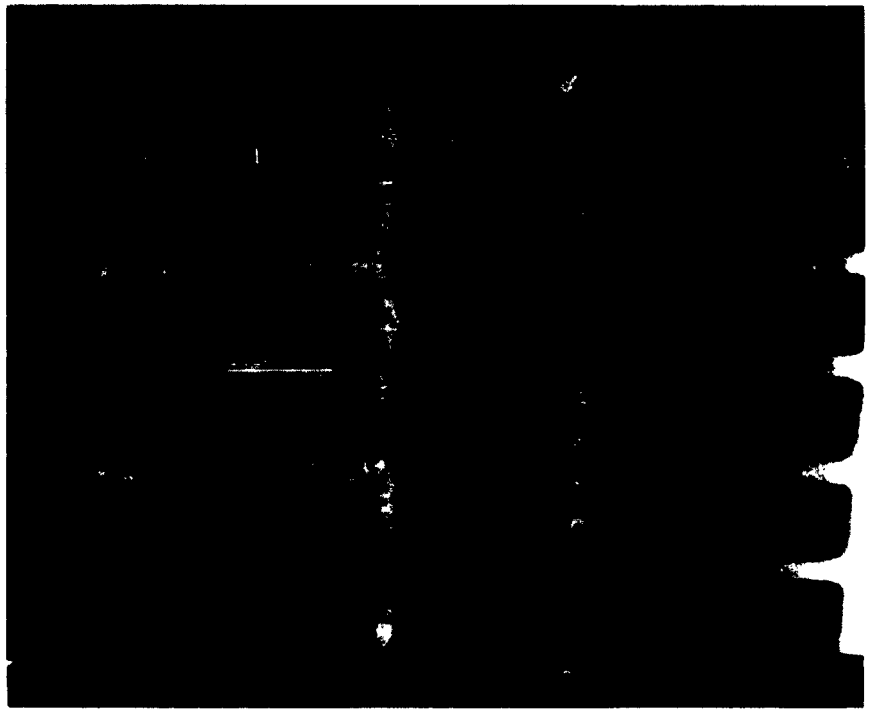


FIGURE 4.17 Over-etched copper plating in a small hole.

BY_____ DATE_____ SUBJECT FINE LINE ETCHING SHEET NO. 6 OF 8

CHKD. BY [illegible] DATE 12/12 DATA SHEET JOB NO. 898

CU (OZ)	PATTERN SIZE	ETCH TYPE	AFTER ETCHING LINE WIDTH (MICROMETER DIVISIONS) 1	2	3	4	5	CALIBRATION FACTOR	PART NO.
2	.003	TANK		ETCHED	AWAY				239
	.010		833	829	—	—	784	7.68×10^{-6} IN/DIV	240
			852	872	—	—	840		241
			784	800	—	—	769		242
			929	914	—	—	871		243
	.020		1088	1080	1062	1098	1077	15.26×10^{-6} IN/DIV	244
			1093	1051	1043	1121	1091		245
			1164	1108	1085	1135	1127		246
			1118	1076	1056	1120	1109		247
	.003	SPRAY	ETCHED		AWAY				248
	.003		ETCHED		AWAY				249
	.010	FRESH BATH (TIME = 2½ MINUTES)	909	896	1065	1096	918	7.68×10^{-6} IN/DIV	250
			823	868	1115	1133	865		251
			865	878	1010	1178	885		252
			855	894	1080	1022	859		253
			885	918	1065	1069	876		254
			957	946	1143	1132	943		255
			872	939	1271	1079	932		256
			921	929	1164	1221	907		257
			919	926	1154	1182	914		258
			824	838	1042	1102	839		259
	.020		1129	1118	1114	1160	1149	15.26×10^{-6} IN/DIV	260
			1148	1098	1131	1110	1126		261
			1145	1117	1098	1150	1161		262
			1116	1106	1079	1121	1116		263
			1126	1111	1090	1128	1140		264
			1152	1121	1114	1150	1158		265
			1120	1100	1089	1184	1141		266
			1142	1108	1111	1143	1150		267
			1123	1116	1071	1115	1115		268
			1124	1091	1117	1148	1123		269
	.003	SPRAY	ETCHED		AWAY				270
	.003		ETCHED		AWAY				271
	.010	SPENT BATH (TIME = 4½ MIN.)	967	977	1117	1171	997	7.68×10^{-6} IN/DIV	272
			974	968	1214	1188	974		273
			931	977	1203	1162	928		274
			907	936	1171	1164	945		275
			922	936	1166	1170	938		276

BY_____ DATE_____ SUBJECT FINE LINE ETCHING DATA SHEET SHEET NO. 7 OF 8

CHKD. BY KM DATE 12/12 JOB NO. 898

CU (OZ)	PATTERN SIZE	ETCH TYPE	AFTER ETCHING LINE WIDTH (MICROMETER DIVISIONS) 1	2	3	4	5	CALIBRATION FACTOR	PART NO.
2	.010	SPRAY	922	965	1273	1215	936		277
			881	924	1085	1032	854		278
			915	896	1133	1071	867		279
			892	877	1064	1040	875		280
			849	864	1073	1093	840		281
	.020		1130	1080	1100	1166	1135	15.26×10^{-6}	282
			1110	1093	1099	1134	1129	IN/DIV	283
			1100	1093	1095	1123	1120		284
			1117	1067	1049	1097	1089		285
			1141	1123	1097	1144	1153		286
			1153	1106	1108	1153	1159		287
			1151	1138	1139	1168	1177		288
			1152	1113	1135	1172	1150		289
			1140	1130	1100	1131	1136		290
			1108	1098	1054	1100	1100		291

SPENT BATH (TIME = 4 1/2 MINUTES)

BY_____ DATE_____ SUBJECT FINE LINE ETCHING SHEET NO. 5 OF 8

CHKD. BY RM DATE 12/12 DATA SHEET JOB NO. 898

Cu (oz)	PATTERN SIZE	ETCH TYPE	AFTER ETCHING LINE WIDTH (MICRO. DIVISIONS) 1	2	3	4	5	CALIBRATION FACTOR	PART NO.
2	.003	SPRAY	VERY UNEVEN - PARTIALLY ETCHED AWAY					S	201
	.003		291	215	NONE	—	—	S	202
	.010		874	981	1242	1257	894	S	203
	.010		870	891	1274	1116	876	S	204
	.020		1131	1070	1087	1130	1108	L	205
	.020		1056	989	1011	1057	1044	L	206
	.003		PARTIALLY ETCHED AWAY					S	207
	.003		"		"	"		S	208
	.010		440	475	628	728	435	L	209
	.010		474	473	711	671	460	L	210
	.020		1118	1089	1100	1127	1120	L	211
	.003		PARTIALLY ETCHED AWAY					S	212
	.003		"		"	"		S	213
	.010		477	491	706	704	471	L	214
	.010		407	450	555	572	411	L	215
	.020		1116	1111	1121	1157	1139	L	216
	.020		1096	1075	1063	1113	1098	L	217
	.003	SPLASH	VERY UNEVEN - PARTIALLY ETCHED AWAY					S	218
	.003		217	221	204	205	196	S	219
	.010		484	526	683	646	506	L	220
	.010		496	491	681	694	483	L	221
	.020		1186	1162	1147	1179	1171	L	222
	.020		1178	1172	1134	1189	1186	L	223
	.003		PARTIALLY ETCHED THROUGH					S	224
	.003		223	179	175	187	174	S	225
	.010		500	508	719	720	497	L	226
	.010		486	519	754	712	485	L	227
	.020		1154	1122	1138	1178	1148	L	228
	.020		1186	1170	1163	1197	1182	L	229
	.003		192	212	237	227	226	S	230
	.003		ETCHED AWAY					S	231
	.010		501	506	679	699	491	L	232
	.010		495	527	725	714	478	L	233
	.020		1190	1131	1143	1172	1191	L	234
	.020		1171	1144	1122	1161	1155	L	235
	.003	TANK	ETCHED AWAY						236
	.003		ETCHED AWAY						237
	.003		ETCHED AWAY						238

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G. Messner - R.McCaw - M. Palmasek

Second Quarterly Progress Report 15 September to 15 December 1962. pp-Graphs, Signal Corps Contract DA-36-039-SC-90763 Unclassified Report.

In the period covered by this report further investigations were carried out in the preliminary research and development phase of the contract.

Additional data on the etching of thin conductors has been collected, the tolerance limitations and the shapes of the cross sections of the thin etched conductors have been established. The parameters of the variables of the lamination cycle have been determined. The placing of resilient layers between the circuit stack and the jig plates for even pressure distribution during the lamination, has been found desirable. The laminating plates must be manufactured of materials which are stable under repetitive temperature and pressure cycling. A technique for registration of all layers within ± .003" from true position has been developed.

The drilling of small holes in ultraminiature layered printed wiring must be a tightly controlled process in order to obtain uniform clean holes. The use of upside down drilling machines has made it possible to keep the required tolerances on hole locations.

Uniform copper deposition can be achieved in the holes with diameters less than .025" and more than two diameters deep when panel plating technique is used. For plating of such holes in circuit boards without any circuit patterns or lands on either surface, special techniques must be developed.

Unclassified

1) Thin conductor etching

2) Lamination cycles

3) Small hole drilling

4) Microminiature plated-through holes

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